

COMPUTER ABSTRACTS

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GENERAL

621 **The Computer Issue.** H. T. Larson, *Proc. IRE*, **49**, Jan. 1961, 4-7. Introduction to the January 1961 issue of the *Proceedings of the IRE*, which is devoted to computers, by the Guest Editor of the issue. An outline is given of the papers contained in the issue; these papers are abstracted in Refs. 623, 628, 632, 635, 637, 641, 642, 643, 652, 653, 655, 678, 679, 680, 681, 701, 703, 705, 718, 720, 722, 741, 751, 786, 793, 797, 809, 813 and 833.

622 **1960 computer progress.** G. L. Hollander (Ed.), E. Berezin, R. S. Gillett, L. A. Gould, R. R. Johnson, J. H. McLeod, D. Ream, and D. L. Stevens, *Instr. & Control Systems*, **34**, Feb. 1961, 229, 231. Report by Ad Hoc Group of the AIEE Computing Devices Committee, presented at AIEE Winter General Meeting, New York, 30 January 1961. It briefly surveys new computers, application to design, evaluation and simulation, trends in organisation of computer systems, computer control, medical uses, and new techniques and devices.

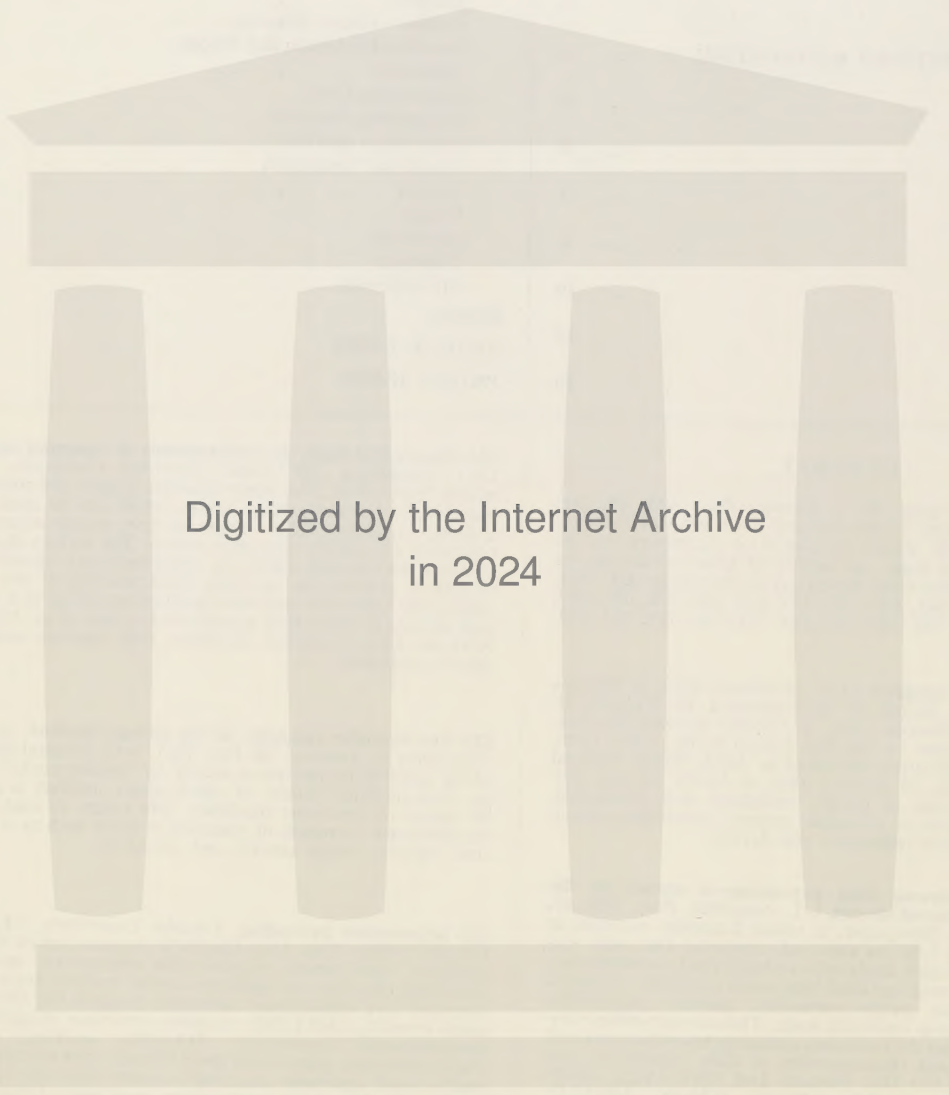
623 **European electronic data processing—a report on the industry and the state-of-the-art.** I. L. Auerbach, *Proc. IRE*, **49**, Jan. 1961, 330-348. This paper, in which European activities in the data processing field are surveyed, comprises two main sections. In the first, which deals with technological developments, the main topics covered are fixed high speed memories, magnetic thin films, random access memories, pattern recognition, machine learning, and hydraulic logic. The second section consists of brief notes on the following computer manufacturers and centres and tabulated characteristics of their computers: Leo Computers Ltd. (LEO III); Ferranti Ltd. (PEGASUS, MERCURY, PERSEUS, SIRIUS, ARGUS, ORION, APOLLO, ATLAS); Elliott Brothers (803, 503); EMI Electronics Ltd. (EMIDEC 1100, EMIDEC 2400); ICT (1200, 1201, 1202, 1301); Standard Telephones & Cables Ltd. (STANTEC ZEBRA, STANTEC Computing System); English Electric (DEUCE, KDF-9); Compagnie des Machines Bull (GAMMA 3, GAMMA 60); Societe d'Electronique et d'Automatisme (CAB 3030, CAB 500, SEA 3900, CAB 5000); Societe Nouvelle d'Electronique (KL 901); University of Pisa (CEP); Olivetti (ELEA 6001, ELEA 9003); Siemens & Halske A.-G. (2002); Telefunken (TR-4); Standard Elektrik Lorenz (ER-56, SEL-B7); Zuse K.-G. (Z-22R, Z-23, Z-31); N.V. Electrologica (X1); N. V. Philips Gloeilampen Fabrieken (PASCAL, STEVIN); Facit (EDB 2, EDB 3); Regnecentralen Dansk Institut for Matematikmaskiner (GIER).

624 **Games that teach the fundamentals of computer operation.** D. C. Engelbart, *IRE Trans. Electronic Computers*, **EC-10**, March 1961, 31-41. This paper describes simple and entertaining exercises of a parlour game nature, which can be used to give a group of laymen some insight of how simple elements are organised in a digital computer system. The laymen themselves simulate the elements which are organised into a network. Each individual watches the up-down hand position of one or two others, and adjusts his own hand position according to a response task allotted to him which is equivalent to that of an AND, OR, NOT or flip-flop element. Counters, shift registers and adders may be organised.

625 **The scientific extension of the human intellect.** S. Ramo, *Computers & Automn.*, **10**, Feb. 1961, 9-12. General discussion of the possibilities offered to society by "intellectronic" systems, i.e. man-machine systems in which man's intellect is extended by means of electronic machines. The effects of such systems are illustrated by means of examples in fields such as law, medicine, banking, traffic control and education.

626 **Information processing.** Lincoln Laboratory, M.I.T., *PB 150602*, 15 June 1960, 56 p. Quarterly progress report. Contents: computer development; magnetic film engineering; information processes; character recognition; current-operated logic circuits; magnetic core applications; computer program for Morse automatic decoding (MAUDE); magnetic materials; magnetic films; semiconductor components; MAUDE; learning; linguistic studies; transient queues with finite storage; on a system of integrodifferential equations occurring in reactor dynamics; sequences and residue class rings; some further properties of Bose-Chaudhuri codes, man-machine communications; human information processing. 16 refs.

627 **Multiple task study on automatic data processing.** R. O. Lucier, H. J. Gray et al., University of Pennsylvania, *PB 152989*, 31 March 1960, 71 p. An account is given of the increasing difficulty of obtaining programmers and the problems expected to arise in this field are stated. The model for the nerve cell construction is discussed on a sounder basis. Extended machine programming is continued, with emphasis on the control of sequences by the allocation interpreter. 2 refs.



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DESIGN

628 Arbitrary Boolean functions of N variables realizable in terms of threshold devices. O. B. Stram, *Proc. IRE*, **49**, Jan. 1961, 210-220. This paper presents a method for the logical design of single stage, combinatorial switching circuits of n variables. The method is applicable to circuits composed of threshold devices such as magnetic cores, transistors with Kirchhoff adder inputs, parametrons, etc. A study of the constraints imposed by the form of the input portions of the threshold devices leads to the definition of certain classes of functions which are physically realisable in a single device. By means of this method, arbitrary Boolean functions of as many as seven variables have been easily designed by hand computations. 5 refs.

629 Axiomatic majority-decision logic. M. Cohn and R. Lindaman, *IRE Trans. Electronic Computers*, **EC-10**, March 1961, 17-21. In this paper, a new algebra, formally independent of Boolean algebra, for logical design with majority-decision elements (parametrons, Esaki diodes, etc.) is derived formally from a set of axioms. The algebra is limited to networks of three-input binary majority-decision elements having no memory loops. The algebra is used to derive design equations for a full binary adder. 5 refs.

630 Bilateral switching using nonsymmetric elements. M. Aoki, and G. Estrin, *IRE Trans. Electronic Computers*, **EC-10**, March 1961, 42-50. A number of different configurations have been proposed permitting bipolar drive currents in magnetic memory elements. This paper is concerned with a configuration which has been investigated and applied in a word organised memory at the University of California. It consists of a pair of mutually inverted and parallel connected transistors which are not, in general, symmetrical. The characteristics of the inverted pair in terms of the current division between the two transistors and the maximum of the power dissipation in the two transistors are discussed, and the critical base current is shown to be the most significant parameter in deciding the maximum power dissipation. A design procedure to determine the possible transistor-parameter ranges for which this current stays less than a specified value is given. 3 refs.

631 Boolean functions realizable with single threshold devices. C. K. Chow, *Proc. IRE*, **49**, Jan. 1961, 370-371. Letter presenting a different approach to the problem discussed in a letter of the same title by M. C. Paull and E. J. McCluskey, *ibid*, **48**, July 1960, 1335-1337 (*C.A.*, **5**, March 1961, Ref. 427).

632 Calculated waveforms for tunnel diode locked pair. H. R. Kaupp and D. R. Crosby, *Proc. IRE*, **49**, Jan. 1961, 146-154. After outlining the basic concepts of tunnel diode locked pair circuitry for computer logic, this paper presents and discusses voltage and current waveforms calculated with a digital computer. 5 refs.

633 Code conversion by NOR logic. J. M. Boswell, *Instr. & Control Systems*, **34**, Feb. 1961, 254-255. Brief account of functioning of a binary-to-decimal converter employing 14 NOR elements.

634 Combined latch-trigger circuit. S. Pitkowski, *IBM Technical Disclosure Bull.*, **3**, Feb. 1961, 20. Brief description of a circuit which stores an input signal in a trigger at any time except during a sampling interval when the state of the trigger is latched.

635 A computer subsystem using kilomegacycle subharmonic oscillators. I. Abeyta, F. Borgini and D. R. Crosby, *Proc. IRE*, **49**, Jan. 1961, 128-135. This paper describes and discusses a computer subsystem which has been constructed employing subharmonic oscillators driven with a 3.7 kMc/s sine wave source. A three-phase power supply is modulated at a 30 Mc/s rate so the interval between successive logic operations is 11 nsec. The logic module is a balanced resonant varactor circuit having a pulsed subharmonic output at 1.8 kMc/s and a rise time of 3 nsec. The output from each module is distributed through a network of resistors and coaxial lines to the modules of the succeeding power supply phase. The logic is done at 1.85 kMc/s by forming a majority of three from the three inputs. The power supply consists of a klystron oscillator supplying a CW signal to the hybrid modulator. The nonlinear element in the modulator is a varactor, which is also driven by a 30 Mc/s trapezoidal wave having a 3 nsec rise time. The modulator output, of 150 mw peak, is amplified by a travelling wave tube to yield the single phase supply of 6 watts, which is converted to the three-phase supply by a three-way power splitter having three transmission lines of lengths differing by 11 nsec. The subsystem contains a three-phase ring, two majority gates, and their majority logic drivers, comprising a total of seven subharmonic oscillators. Operation is stable, with reasonable allowable variations in the power supply frequency and amplitude. 10 refs.

636 Correction. *IRE Trans. Electronic Computers*, **EC-10**, March 1961, 62. Correction of typographical errors in "Minimization of contact networks subject to reliability specifications", A. Gill, *ibid*, **EC-9**, March 1960, 25-29 (*C.A.*, **4**, August 1960, Ref. 1397).

637 Developments in the logical organization of computer arithmetic and control units. F. S. Beckman, F. P. Brooks and W. J. Lawless, *Proc. IRE*, **49**, Jan. 1961, 53-66. This paper reviews development during recent years and indicates current trends in the organisation of basic components into "packages" that perform arithmetic and control functions. The characteristics of physical devices which influence the speed and design of circuitry and the micro-level of logical organisation are not considered. The main sections of the paper deal with addressing and address modification, sequencing and control, arithmetic and logical operations, and input-output control. 60 refs.

638 A digital correlator based on the residue number system. P. W. Cheney, *IRE Trans. Electronic Computers*, **EC-10**, March 1961, 63-70. After briefly reviewing various devices for the calculation of correlation functions, the advantages of the residue number system for a digital correlator are indicated, and the implementation of residue number logic is discussed. The system design of a digital correlator based on the residue number system is then presented. 21 refs.

639 Electronic commutator. T. G. Floros and D. S. Grubb, *IBM Technical Disclosure Bull.*, **3**, Feb. 1961, 23-24. Brief description of a clock circuit providing sequential but separate outputs that number up to twice the number of trigger circuits used.

640 Ferrite toroid core circuit analysis. R. Betts, and G. Bishop, *IRE Trans. Electronic Computers*, **EC-10**, March 1961, 51-56. This paper presents an analysis of the terminal characteristics of thin ferrite toroid cores under arbitrary drive and load conditions. The analysis is founded only on the following two experimentally confirmed conditions: the time required for a complete reversal of flux under unloaded conditions is inversely proportional to the magnitude of a step-driving field which is in excess of the critical field required to initiate flux change; and the open circuit voltage-time output waveforms caused by step driving currents are identical when normalised with respect to amplitude and time. The normalised output voltage waveform is used to develop a terminal characteristic equation. Equations are developed to allow the prediction of core response to arbitrary input waveforms. The equations are expanded to include a load circuit and to test the validity of the expressions developed. Theoretical and experimental results are compared for a core loaded with series RL and RLC circuits with both ramp and step-drive currents. 4 refs.

641 Flow table logic. P. R. Low and G. A. Maley, *Proc. IRE*, **49**, Jan. 1961, 221-228. Micro-miniature systems have been proposed which will use packing densities of the order of 10^6 active elements per cubic foot. In order to deal with the problem of interconnecting these elements, it has been suggested that the logic and organisation of a computer system should be re-examined. Such a re-examination might lead to a new system of logic and, perhaps, a complete new theory of machine organisation. This paper represents the results of one such study with the ultimate objective of treating a computer as a single sequential circuit. It is thought that the concept presented in the paper whereby large sequential circuits are implemented directly from their flow table representations may contribute to the efficient utilisation of the so-called batch-fabricated devices. A technique for designing sequential circuits due to D. R. Huffman is first outlined. In this technique a chart, called a "flow table" is used to record past input conditions and to define the operation of the desired circuitry. The vertical columns of the chart are labelled to indicate all possible input conditions and the horizontal rows all possible conditions of the memory elements within the circuitry. The new technique provides a basic configuration consisting of a grid of conductors having insulated crossings, the vertical conductors being related to the columns and the horizontal conductors to the rows of the flow table. Two types of active elements are used; one is a "conditional latch" and the other is a transfer element which is used as an AND circuit. The conditional latch is placed at the intersection of a column and a row in a position corresponding to the position of the stable state in the flow table and information is transmitted from it to all other elements connected on the same row. The function of the transfer element is to transfer a logical "1" from the horizontal buss vertically to a particular latch. A circuit designed using flow table logic is extremely regular which is an advantage for micro-miniature, or molecular electronic, systems. 4 refs.

642 **High density digital magnetic recording techniques.** A. S. Hoagland and G. C. Bacon, *Proc. IRE*, **49**, Jan. 1961, 258-267. Reprinted from *IRE Trans. Electronic Computers*, **EC-9**, March 1960, 2-11. For abstract see *C.A.*, **4**, August 1960. Ref. 1394.

643 **High-speed arithmetic in binary computers.** O. L. MacSorley, *Proc. IRE*, **49**, Jan. 1961, 67-91. This paper considers from the viewpoint of the systems designer, various methods of increasing the speed of performing the basic arithmetic operations. Methods of obtaining high speed in addition, multiplication and division in parallel binary computers are described and then compared with each other as to efficiency of operation and cost. The transit time of a logical unit is used as a time base in comparing the operation speeds of different methods, and the number of individual logical units required is used in the comparison of costs. The methods described are logical and mathematical, and may be used with various types of circuits. Application to a computer is clarified by means of examples in which specific circuit types are assumed. 11 refs. See also Ref. 652.

644 **On internal variable assignments for sequential switching circuits.** R. Bianchini and C. Freiman, *IRE Trans. Electronic Computers*, **EC-10**, March 1961, 95-96. Letter referring to "A note on the number of internal variable assignments for sequential switching circuits", E. J. McCluskey and S. H. Unger, *ibid.*, **EC-8**, Dec. 1959, 439-440 (*C.A.*, **4**, July 1960, Ref. 1100). In that paper there was developed the number of nondegenerate equivalence classes of state assignments which exist when v binary variables are used to designate r states. In this letter, a method is presented of obtaining a representative of each of these nondegenerate equivalence classes which does not require that any pair of assignments ever be tested for equivalence.

645 **Linear-input logic.** R. C. Minnick, *IRE Trans. Electronic Computers*, **EC-10**, March 1961, 6-16. This paper is concerned with techniques for the logical design of magnetic core circuits to produce arbitrary single-output combinational switching functions. The approach is based on the relationship of a single magnetic core circuit to a linearly separable switching function. A synthesis procedure is developed which uses a pair of logical primitives, AND with NOT and OR with NOT, which are similar to the STROKE primitive and its inverse. Procedures are developed for the synthesis of symmetric functions which require no more than the integral part of $(n+3)/2$ cores, approximately half the number used in previously published procedures. The synthesis of arbitrary switching circuits is treated as a linear programming problem, and a table of all four-variable circuits is presented in which no circuit requires more than three cores. 25 refs.

646 **A magnetic core code-validity checking circuit.** E. B. Eichelberger, *IBM Technical Disclosure Bull.*, **3**, Feb. 1961, 37. Brief description of a magnetic core circuit for indicating an error in an m out of n type code.

647 **Majority gates applied to simultaneous comparators.** H. S. Miller, *IRE Trans. Electronic Computers*, **EC-10**, March 1961, 94-95. This letter points out an application of majority gates to a simultaneous comparator net. By "simultaneous", it is inferred that simultaneous answers to the questions $Is X > Y?$; $Is X = Y?$; and $Is X < Y?$ will appear at the output of the net. 7 refs.

648 **NAND logic clock.** H. J. Zentgraf, *IBM Technical Disclosure Bull.*, **3**, Feb. 1961, 21. Brief description of a clock circuit employing NAND (not-AND) gates, which produces a timed sequence of pulses at six separate outputs. See also Ref. 649.

649 **NAND logic clock.** H. J. Zentgraf, *IBM Technical Disclosure Bull.*, **3**, Feb. 1961, 22. Brief description of a clock circuit, employing NAND (not-AND) gates, which provides eight sequential outputs. See also Ref. 648.

650 **Self-repairing computers.** M. V. Wilkes, *IRE Trans. Electronic Computers*, **EC-10**, March 1961, 93-94. Letter suggesting a possible way of setting up a self-repairing computer. Briefly, a very large collection of flip-flops, AND gates and OR gates would be interconnected to form a random net in which a computer specified by a given block diagram would be selected by an auxiliary computer which would check to avoid faulty elements.

651 **A simple synchronising circuit.** R. C. McGuire, *IBM Technical Disclosure Bull.*, **3**, Feb. 1961, 19. Brief description of logic circuitry which synchronises pulses produced at randomly occurring times with standard clock pulses.

652 **Statistical analysis of certain binary division algorithms.** C. V. Freiman, *Proc. IRE*, **49**, Jan. 1961, 91-103. This paper is concerned with the statistical analysis of the nondeterministic extensions of the nonrestoring method of binary division described in Ref. 643. One extension requires that the magnitudes of the divisor and partial remainders be "normal", i.e. in the range $[0.5, 1.0)$. This leads to a time improvement of more than two relative to conventional nonrestoring methods. Other extensions involve the use of several divisor multiples (or trial quotients). A Markov chain model is used to analyse this method. Steady-state distributions are determined for the division remainder and performance figures based on both this steady-state distribution and a random distribution are calculated. These are compared with the results of a computer simulation of 2^{14} randomly-chosen division problems using two specific methods of division. 9 refs.

653 **Statistical analysis of logic circuit performance in digital systems.** E. Nussbaum, E. A. Irland and C. E. Young, *Proc. IRE*, **49**, Jan. 1961, 236-244. The overall performance of a digital system containing large numbers of relatively few basic circuit configurations is largely limited by the characteristics of these building block circuits. This paper propounds the thesis that if these characteristics (speed, logical gain, noise margin) are treated on a statistical basis, as opposed to a worst case approach, substantial improvements in logical design flexibility may be attained, and treats the problem of obtaining the statistical distribution of the response or output of some circuit as a function of the distributions of individual component parameter variations. The approach is that of an engineering solution to the problem, rather than a rigorous statistical treatment. A brief survey is given of the methods of analysis for the combination of frequency curves; an algebraic method based on a Taylor series expansion which is suitable for hand calculation and a numerical (Monte Carlo) method suitable for machine computation are considered. Transistor resistor logic circuits are then analysed in more detail. Resultant distributions of propagation delays and logical gain are obtained as functions of circuit parameter distributions, logical configuration and temperature. Finally, there is a discussion of how the results may be used by logic and system designers and the effect of the statistical analysis on system reliability and cost figures. 13 refs.

654 **Subharmonic generation with nonlinear reactance—a circuit analysis.** D. B. Leeson, *Proc. IRE*, **49**, Jan. 1961, 351-352. This letter presents a circuit analysis of subharmonic generators employing nonlinear reactance, the approach being similar to that used successfully in the analysis of harmonic generators. 2 refs.

655 **A survey of tunnel-diode digital techniques.** R. C. Sims, E. R. Beck and V. C. Kamm, *Proc. IRE*, **49**, Jan. 1961, 136-146. This paper is concerned with the use of the tunnel diode in memory and logic circuitry and discusses the major techniques that have been reported together with some that have been developed by the authors and others at the Bendix Research Laboratories. After briefly considering the major characteristics of tunnel diodes, various memory circuits are described with particular attention to random access matrices. The principles of tunnel diode logic design are illustrated by means of basic threshold circuits and OR, AND, NOT and other logic circuits are described. 10 refs.

656 **Unate truth functions.** R. McNaughton, *IRE Trans. Electronic Computers*, **EC-10**, March 1961, 1-6. This paper contains some applications of an elementary study of unate truth functions. One application is a method of deciding when a truth function is linearly separated, i.e. is expressible as a linear polynomial inequality in its arguments (letting 1 represent truth and 0 represent falsity). Other applications are to contact nets and to rectifier nets. 12 refs.

657 **Inertial selection for magnetic core logic.** R. H. Tancrell, M.I.T., *PB 152637*, 11 Oct. 1960, 29 p. With the inertial selection scheme, logical functions can be performed by connecting toroidal ferrite cores together with single turn windings only. A "flux gain" feature is thereby obtained which allows more flux to be switched into a receiving core than is received there from a transmitting core. To achieve these characteristics the inertial selection scheme utilises two thresholds of low coercive force ferrite cores. It also uses the property that one of these thresholds can be changed by electrical means. In this report detailed discussions are given of the factors involved in understanding these magnetic characteristics and their utilisation in logic applications. 11 refs.

658 Test of a model dynamic system synthesizer. R. C. Mikulich, University of Chicago, *PB 171144*, Feb. 1958, 175 p. A mathematical (as opposed to engineering) test programme, conducted in conjunction with a programme to design and develop performance tests for continuous computers and involving unique tests, was effected to test an experimental eighteen-amplifier analogue computer developed by the Radio Corporation of America. This report is an account of that test programme and includes a comprehensive analysis of the components, a full account of the system tests, a discussion of individual system and results, and a presentation of operational aspects. 7 refs.

659 Pulse shaping circuit. Electric & Musical Industries Ltd., *B.P. 860225*, 1 Feb. 1961. A pulse shaping circuit for digital computers is supplied with timing pulses and employs two valves or transistors which are alternatively conductive and two diodes.

660 Binary division circuit. Monroe Calculating Machine Co., *B.P. 860852*, 8 Feb. 1961. A binary divider for division by integers other than powers of two, comprises two adder-subtractor circuits; the output of one of these circuits is connected to the input of the other circuit and the output of such other circuit is connected, through means for delaying by an integral number of pulse times, to inputs of both circuits.

661 Magnetic core circuitry. Soc. d'Electronique et d'Automatisme, *B.P. 861658*, 22 Feb. 1961. Magnetic core circuitry for handling binary data employs cascade connected cores with improved interconnecting networks.

662 Digital function evaluation. Electric & Musical Industries Ltd., *B.P. 861680*, 22 Feb. 1961. The arithmetic of digital computers is simplified by means of a digital function evaluator in which gates are selectively opened and closed to cycle signals from storage means through a two-input, one-output logical element to enable several logical functions to be evaluated.

663 Control circuitry for ferrite apertured plate memory. Int. Business Machines Corp., *B.P. 861688*, 22 Feb. 1961. Current control circuitry, specially designed for driving and selection purposes with ferrite apertured plate memories, includes two current sources and several transformers each of which has two windings connected between the sources and a common point.

664 Floating decimal system. Int. Business Machines Corp., *U.S.P. 2951637*, 6 Sept. 1960. This patent is concerned with a floating decimal system in which improved circuit arrangements, including an adder and a delay device, are provided for shifting data in some orders of a storage device while adding to another order without a shift.

665 Data transfer circuitry. Burroughs Corp., *U.S.P. 2952007*, 6 Sept. 1960. Reliable, noise-free transfer of data between magnetic cores is obtained with a circuit which includes an air-cored inductor.

666 Reading circuitry for magnetic core matrices. Radio Corp. of America, *U.S.P. 2952838*, 13 Sept. 1960. A reading circuit for a coincident-current magnetic core memory, in which the output of an integrator is applied directly and through delay means to a differential amplifier.

667 Selection system for magnetic core matrix. U.S. Secretary of Commerce, *U.S.P. 2953774*, 20 Sept. 1960. Selection of cores in a storage matrix is effected with the aid of two gate cores associated with each storage core.

668 Check digit monitoring and correcting circuits. Int. Business Machines Corp., *U.S.P. 2954164*, 27 Sept. 1960. This patent describes circuitry whereby a new check digit for a word is computed by arithmetically combining the current check digit and a correction factor derived from changes in the word, without examining unchanged portions of the word.

669 Clock pulse generator. Int. Business Machines Corp., *U.S.P. 2955254*, 4 Oct. 1960. This patent is concerned with a pulse generator designed to produce a series of accurately-timed, overlapping pulses.

670 Ferroelectric switching matrices for driving a ferroelectric storage matrix. Int. Business Machines Corp., *U.S.P. 2955281*, 4 Oct. 1960. An arrangement employing row and column ferroelectric switching matrices to enable individual ferroelectric capacitors in a storage matrix to be addressed an indefinite number of times without disturbing data stored on other capacitors of the matrix.

671 Checking of serial, binary-decimal words. Int. Business Machines Corp., *U.S.P. 2955756*, 11 Oct. 1960. This patent concerns circuit arrangements for checking if a word expressed in binary-decimal notation and its check digit are in agreement. On receipt of a check digit, a ring counter is advanced to a position corresponding to the decimal value of the digit. Thereafter, as each digit of the word is received the counter is advanced one position for each bit present in each digit. After all the digits have been received, the counter stands at a predetermined position if the check digit and the word are in agreement.

672 Gating system for parametron computers. Kokusai Denshin Denwa K.K., *U.S.P. 2956173*, 11 Oct. 1960. Circuit arrangements for selective transmission of digital signals through parametrons, in channel selecting and shift register circuits, by controlling the oscillation of the parametrons with a gating signal.

673 Checking circuit for a decoder matrix. Int. Business Machines Corp., *U.S.P. 2958072*, 25 Oct. 1960. A circuit arrangement of OR and EXCLUSIVE OR circuits is employed to check the proper operation of the AND circuits in a decoder matrix.

See also :—

General, Ref. 626.

Techniques, Ref. 705.

Applications: Electronics, Ref. 812.

LEARNING AND PATTERN RECOGNITION

674 Further results on the N-tuple pattern recognition method. W. W. Bledsoe, *IRE Trans. Electronic Computers*, **EC-10**, March 1961, 96. Letter referring to the pattern recognition method described by the author and I. Browning (see *C.A.*, **4**, July 1960, Ref. 1200) and briefly reporting the results of an extension of the tests described by W. H. Highleyman and L. A. Kametsky (see *C.A.*, **4**, Sept. 1960, Ref. 1700). See also Refs. 675 and 676.

675 A possibly misleading conclusion as to the inferiority of one method for pattern recognition to a second method to which it is guaranteed to be superior. L. Uhr, *IRE Trans. Electronic Computers*, **EC-10**, March 1961, 96-97. Letter criticising the tests by Highleyman and Kametsky of the Bledsoe and Browning pattern recognition method. See also Refs. 674 and 676.

676 Further comments on the N-tuple pattern recognition method. W. H. Highleyman, *IRE Trans. Electronic Computers*, **EC-10**, March 1961, 97. Letter commenting on the letters abstracted in Refs. 674 and 675.

677 Optimum performance of learning machines. A. Gamba, *Proc. IRE*, **49**, Jan. 1961, 349-350. A letter in which, after defining "learning" as the ability of making correct assignments or statements as if the machine had guessed a rule, the following basic principle is stated: Every learning machine, no matter how "intelligent", cannot outperform a mathematician, using probability theory at its best, and having the same information. This principle is then applied to the perceptron. 4 refs.

678 Pattern recognition using autocorrelation. L. P. Horwitz and G. L. Shelton, *Proc. IRE*, **49**, Jan. 1961, 175-185. This paper is concerned with certain techniques for character recognition characterised by a particular manner of dealing with character misregistration. The basic idea underlying the techniques is that of registration invariance, i.e. all patterns are described in such a way that shifting translationally in any direction does not affect any observed parameter. In the first section of the paper the registration invariant mathematical formalism is given. The starting point is the construction of a discrete binary representation of the patterns to be recognised. This is done, in principle, by placing a discrete mesh over the character and setting each mesh point to unity if it covers a black part of the character and to zero if it covers white. The patterns are then described by counting specified pairs of ones regardless of their positions in the matrix for all possible kinds of pairs. The second section of the paper describes several recognition schemes as physical realisations of the mathematical operations. 8 refs.

679 Self-organizing systems—a review and commentary. J. K. Hawkins, *Proc. IRE*, **49**, Jan. 1961, 31-48. This paper is concerned with self-organising machines, i.e. machines containing a variable network in which the elements are organised by the machine itself to meet criteria of successful operation, and has the object of summarising significant work, generalising upon it and evaluating its status. A historical review is given of the class of self-organising systems represented by networks which learn to recognise patterns and some behavioral similarities between such networks and biological nervous systems are discussed. Examples and results of several experimental models for alpha-numeric character recognition are presented. The network synthesis problem is recast in terms of redundant information removal, multivariable curve fitting and expansion in orthonormal functions, and recognition network structures and the learning process are described from these points of view. The potential component and behavioral advantages to be gained from sequential feedback networks are briefly considered. 60 refs.

680 The simulation of neural elements by electrical networks based on multi-aperture magnetic cores. A. E. Brain, *Proc. IRE*, **49**, Jan. 1961, 49-52. After a brief discussion of multilevel storage, gating, controlling threshold level and summation as basic functional operations common to several systems for the simulation of neural behaviour by electrical networks, it is shown how these operations may be realised very efficiently with multi-apertured magnetic cores. As an example there is described a circuit with threshold control of three simultaneous gates and non-destructive analogue readout which requires only two ferrite cores of the MAD type. 6 refs.

681 Steps towards artificial intelligence. M. Minsky, *Proc. IRE*, **49**, Jan. 1961, 8-30. In this paper the author reviews work directed towards the construction of artificial intelligence and gives his own overall view of the problems involved. The problems of heuristic programming—of making computers solve really difficult problems—are divided into five main areas, which constitute the main sections of the paper: Search, Pattern Recognition, Learning, Planning and Induction. The author summarises the argument presented in the paper as follows: "A computer can do, in a sense, only what it is told to do. But even when we do not know exactly how to solve a certain problem, we may program a machine to *Search* through some large space of solution attempts. Unfortunately, when we write a straightforward program for such a search, we usually find the resulting process to be enormously inefficient. With *Pattern-Recognition* techniques, efficiency can be greatly improved by restricting the machine to use its own methods only on the kind of attempts for which they are appropriate. And with *Learning*, efficiency is further improved by directing Search in accord with earlier experiences. By actually analyzing the situation, using what we call *Planning* methods, the machine may obtain a really fundamental improvement by replacing the originally given Search by a much smaller, more appropriate exploration. Finally, in the section on *Induction*, we consider some rather more global concepts of how one might obtain intelligent machine behavior." The discussion is supported by extensive citation of the literature and by descriptions of a few of the most successful problem-solving programs constructed so far. 95 refs.

682 Computation, behaviour, and structure in fixed and growing automata. A. W. Burks, University of Michigan, *PB 149673*, March 1960, 34 p. Contents: Structure, behaviour, and computation in fixed automata and generalized Turing machines; Analysis and synthesis of automata; Growing automata; Some problems concerning growing automata. 26 refs. (N.B.—For an earlier report see *C.A.*, **5**, Feb. 1961, Ref. 241).

683 Dynamic programming approach to a final-value control system with a random variable having an unknown distribution function. M. Aoki, California University, *PB 149136*, Feb. 1960, 41 p. Given a criterion of performance, the duration of the process and the domain of the control variable, a sequence of control variables $\{v_n\}$ is determined as a function of the state vector of the system and time. The functional equation technique of dynamic programming is used to derive a recurrence relation of the criterion function of the process $k_n(x, z)$ where x is the state variable of the system when there remain n control stages. A concept of suboptimal policy is introduced and numerical experiments are performed to test suboptimal policy suggested from numerical solution. The system behaviour under the suboptimal policy is also discussed. 18 refs.

684 Dynamic programming and numerical experimentation as applied to adaptive control systems. M. Aoki, California University, *PB 147651*, Feb. 1960, 222 p. Solutions of a class of adaptive control systems, especially those similar to the Two Armed Bandit problems, are formulated and discussed. Attempts are made to incorporate some of the ideas of statistical decision theory, dynamic programming and numerical experimentations to provide a more flexible formulation of problems of analysis and synthesis of adaptive control systems. The method used consists of setting up mathematical models, simplifying them so that they admit analytic solutions, and using some approximating analytic or numerical techniques. Using dynamic programming as the main tool of the investigation, discrete deterministic and stochastic control systems are formulated as multi-stage decision processes. Control systems with random inputs are taken up; they are called adaptive control processes. Computational procedures of solving recurrence relations are presented and examples given. 33 refs.

685 Jenny: an improved homeostat. G. G. Haroules and P. F. Haire, Air Force Cambridge Research Center, *PB 152202*, April 1960, 31 p. An improved and enlarged model of Ashby's homeostat is described, in which conventional 60-cycle electro-mechanical analogue computer techniques are used instead of the original d.c. techniques, the number of elements available as main variables is increased from four to sixteen, and provisions are made for electrical command (data) inputs and main variable outputs. 10 refs.

686 The realization of biological computers. H. von Foerster, University of Illinois, *PB 148290*, 15 April 1959, 28 p. Contents: Topology of neural nets—Reliability; General elementary component—General neuron; The Bulbar Plexus; Comments on the logical and mechanical character of elements in a self organizing system—Abstract model, Detailed specifications, Self recognition, Inhibitory control, The set of elements, Signal network, Connection matrix, Energetic structure; An allegory for excitable tissue.

687 A self-organizing binary system. R. Mattson, Lockheed Aircraft Corp., *PB 149652*, Sept. 1959, 30 p. A precise model for an adjustable logical device and a convergent iterative adjustment procedure is presented and analysed. Four demonstrations are given to synthesize optimum logical functions for pattern recognition problems containing from 25 to 216 binary variables. These problems were simulated on the IBM 704, and each problem required less than two minutes of computer time to synthesize an optimum truth function for the process considered. 4 refs.

688 Recognition of handwritten characters. A. J. Betts, *B.P. 860254*, 1 Feb. 1961. A composite signal is produced from a handwritten character traced by a writing member on a surface which includes sensing elements co-operating with the writing member to produce signals, the sensing elements being shaped and arranged so that a significant composite signal is formed for each character.

689 Character recognition. Solartron Electronic Group Ltd., *B.P. 860568*, 8 Feb. 1961. This patent is concerned with electronic reading apparatus designed to permit reading to take place at several locations without duplication of the entire equipment. Scanning means are provided at each of the locations and are coupled by switchable channels to signal storage means and a logical matrix provided at a centralised control location.

690 Character recognition—magnetic ink characters. Int. Business Machines Corp., *B.P. 861555*, 22 Feb. 1961. This patent is concerned with a multi-channel magnetic transducer assembly which is suitable for use in the sensing of magnetic ink characters. Spaced parallel cores are disposed between endplates with the flux path of each core at right angles to the flux paths of adjacent cores.

691 Recognition of magnetic ink characters. Int. Business Machines Corp., *U.S.P. 2955277*, 4 Oct. 1960. In a system for reading characters printed with magnetic ink, flux density variations of different frequencies are recorded on different portions of a character. On subsequent sensing of the character, signals from the different portions are routed to different channels by frequency-selective arrangements.

See also:—

General, Ref. 626.

Applications: Control—Production and Process, Ref. 811.

692 **Bemerkungen zur numerischen Integration gewöhnlicher Differenzialgleichungen n-ter Ordnung.** (Remarks on the numerical integration of ordinary differential equations of the n th order). H. Rutishauser, *Numerische Mathematik*, **2**, 12 Oct. 1960, 263-279. (In German) This paper compares the accuracy of numerical integration of n th order ordinary differential equation by transforming it into a system of n first order differential equations with direct methods using formulae such as the Kutta-Nystrom, Kutta-Zurmuhl and Adams-Falkner formulae. 7 refs.

693 **Bestimmung der Eigenwerte des allgemeinen Eigenwertproblems.** (Determination of eigenvalues for the general eigenvalue problem). H.-L. Haas, *Numerische Mathematik*, **2**, 12 Oct. 1960, 341-353. (In German) This paper presents a procedure for range-maintaining but dimension-reducing transformation of the general eigenvalue problem to the special eigenvalue problem. 2 refs.

694 **A numerical study of Weber's real class number calculation. Part I.** H. Cohn, *Numerische Mathematik*, **2**, 12 Oct. 1960, 347-362. This paper describes a numerical study, using GEORGE, of the class number calculation which arose in Weber's proof of Kronecker's theorem that each abelian field over the rationals is a sub-field of a field generated by some root of unity. 7 refs.

695 **The singularities of the Riemann function.** D. Ludwig, AEC Computing and Appld. Maths. Center, New York University, *AEC Res. & Dev. Report NYO-9351*, 1 Jan. 1961, 86 p. This report deals with the Cauchy problem for linear hyperbolic systems of the first order with $n+1$ independent variables. The central problem is the description of the singularities of the Riemann function. This problem provides a key to the mathematical theory of wave propagation, since any solution of the Cauchy problem can be represented in terms of the Riemann function. The analysis of the singularities of the Riemann function also represents a step towards an extension of the method of Hadamard to general linear hyperbolic equations. This method would determine the Riemann function by substitution of a function of the proper form into the differential equation. The analysis also provides an approach to problems involving propagation of waves in media where the characteristics have variable multiplicity, including questions of existence and uniqueness. The principal methods and concepts are drawn from geometrical optics and asymptotic analysis. 17 refs.

696 **Tables for bivariate osculatory interpolation over a Cartesian grid.** H. E. Salzer and G. M. Kimbro, Convair (Astronautics) Division, General Dynamics Corp., 40 p. In this report, formulae are developed for binary polynomials $P(x,y)$ which agree together with the partial derivatives $P_x(x,y)$ and $P_y(x,y)$, with $f \equiv f(x,y)$, $f_x \equiv f_x(x,y)$ and $f_y \equiv f_y(x,y)$ at n specified points. They have the advantage over ordinary bivariate interpolation of packing $3n$ conditions into n points. Explicit formulae or methods are developed for the general 2- to 5-point cases. Tables are presented of binary polynomial coefficient multipliers for interpolating over any square Cartesian grid. 6 refs.

697 **Table of coefficients for obtaining the second derivative without differences.** H. E. Salzer and P. T. Roberson, Convair (Astronautics) Division, General Dynamics Corp., 32 p. This report presents tables of coefficients, computed on an IBM 650, for obtaining the second derivative without using differences. 5 refs.

698 **Tables of osculatory integration coefficients.** H. E. Salzer, D. C. Shultz and E. P. Thompson, Convair (Astronautics) Division, General Dynamics Corp., 1960, 43 p. This report presents tables of coefficients, computed on an IBM 704, for an n -point osculatory quadrature formula which combines interpolation with integration. 10 refs.

699 **Tschebyscheff-Approximationen in kleinen Intervallen. II. Stetigkeitssätze für gebrochen rationale Approximationen.** (Chebyshev approximations in small intervals. II. Stability considerations for truncated rational approximations). H. Maehly and C. Witzgall, *Numerische Mathematik*, **2**, 12 Oct. 1960, 293-307. (In German). 9 refs.

700 **Untersuchungen des Untergruppenverbandes endlicher Gruppen auf einer programmgesteuerten elektronischen Dualmaschine.** (Investigation of sub-group arrangements of finite groups with a store program electronic computer). J. Neubüser, *Numerische Mathematik*, **2**, 12 Oct. 1960, 280-292. (In German) This paper is concerned with a group theory problem and its programming for the Zuse K-G binary computer Z 22. 3 refs.

See also:—

General. Ref. 626.

701 **Algebraic function calculations using potential analog pairs.** M. L. Morgan, *Proc. IRE*, **49**, Jan. 1961, 276-282. A new potential analogue method, its implementation and application are described. In this method, both the magnitude and angle of functions of a complex variable are calculated from their pole-zero plots. The method is based on a pair of "factor analogue" voltage distributions in a complex plane, on which voltage measurements at the zeros and poles of the function are used for the calculation. 9 refs.

702 **An algorithm for constructing feasible schedules and computing their schedule times.** J. Heller and G. Logemann, AEC Computing & Appld. Maths. Center, New York University, *AEC Res. & Dev. Report NYO-9488*, 15 Nov. 1960, 30 p. This report presents an algorithm for the generation of feasible schedules and the computation of the completion times of the job operations of a feasible schedule. Using this algorithm, the distribution of schedule times over the set of feasible schedules—or a subset of feasible solutions—was determined for technological orderings that could occur in a general machine shop. These distributions are found to be approximately normal. Biasing techniques corresponding to "first come first served", random choice of jobs ready at each machine and combinations of these two extremes were used to compute distributions of schedule times. 7 refs.

703 **Cyclic codes for error detection.** W. W. Peterson and D. T. Brown, *Proc. IRE*, **49**, Jan. 1961, 228-235. In this paper cyclic codes are defined and described from a new viewpoint involving polynomials. The basic properties of Hamming and Fire codes are derived. The potentialities of these codes for error detection and the equipment required for implementing error detection systems using cyclic codes are described. 15 refs.

704 **Some problems in linear graph theory that arise in the analysis of the sequencing of jobs through machines.** J. Heller, AEC Computing & Appld. Maths. Center, New York University, *AEC Res. & Dev. Report NYO-9487*, 15 Oct. 1960, 43 p. In this report the problems of sequencing jobs through machines are discussed in a linear graph framework. The construction of feasible schedules from given technological orderings is related to the construction of transitive graphs from given component graphs. Methods of constructing transitive graphs are given and bounds on the number of different transitive graphs constructed from given components are determined. A recursive convex function defined on the transitive graphs—the job operation completion time and schedule time—is studied. Bounds on the number of different values that the schedule time can attain are obtained. Examples of multi-programming, flow shop and machine shop scheduling are studied. 15 refs.

705 **Transient analysis of cryotron networks by computer simulation.** M. K. Haynes, *Proc. IRE*, **49**, Jan. 1961, 245-257. A general method is derived for transient analysis of complicated nonlinear dynamical systems by use of a digital computer programmed to perform tensor transformations and numerical integration. Tensor methods, adapted from Kron's techniques, are used for converting circuit data into a form for transient simulation by numerical integration. An IBM 704 program for simulation of lumped inductive-resistive circuits consisting of cryotrons is briefly outlined. The results are described in some detail of using this program to study switching speeds of cross-latched cryotron flip-flops; five-stage, free-running, ring circuits; and a three-bit, self-timing, self-checking, binary, parallel adder containing 233 circuit elements including 93 cryotrons arranged in 55 meshes. 4 refs.

706 **On a class of error correcting binary group codes.** R. C. Bose and D. K. Ray-Chaudhuri, University of North Carolina, *PB 148686*, Sept. 1959, 15 p. This report appears to be the same as the paper in *Information & Control*, **3**, March 1960, 68-79 (C.A., **4**, June 1960, Ref. 857). 5 refs.

707 **Compression and coding.** E. Weiss, M.I.T., *PB 152638*, 11 Oct. 1960, 3 p. This report concludes that the search for data compression schemes is the same as a search for error-correcting codes.

708 **Computational chains.** T. Marill and T. G. Evans, Bolt, Beranek and Newman Inc., *PB 152519*, 21 Oct. 1960, 26 p. A formalism is developed within which questions relating to the efficiency of information-manipulative processes may be studied. An example of the application of this theory to the simplification of a computer program is given.

709 Converting beta to b weights on the IBM Type 650. A. Dvorak and C. E. Lunneborg, Washington University, Seattle, *PB 148735*, July 1959, 6 p. This program is designed to scale standard β -prediction weights by appropriate mean and variance estimates, thus generating prediction weights (b weights) suitable for employment with unstandardised predictor observations. The method was specialised to provide the derived weights in a form suitable to be employed with the grade prediction program. 5 refs.

710 An IBM Type 650 program to facilitate obtaining scattergrams. G. R. Burket, Washington University, Seattle, *PB 148734*, July, 1959, 3 p. 1 ref.

711 An IBM Type 650 program for transforming a correlation matrix to be orthogonal to a normalized vector. G. R. Burket, Washington University, Seattle, *PB 148608*, Feb. 1960, 7 p. 2 refs.

712 A method for computing rating scale item statistics on the IBM Type 650. M. M. Campbell, Washington University, Seattle, *PB 148733*, July 1959, 4 p. A modification was made of a fixed-point matrix multiplication routine designed to meet the problem of computing rating scale item statistics with a large number of items. Given frequency data, the program may be used to obtain item means, variances, standard deviations, sums, sums of squares and sums of higher powers. The program performs matrix multiplication augmented by processes for computing means and measures of variability. 1 ref.

713 A modified IBM Type 650 program for a non-symmetric correlation matrix with summed quantities. A. Dvorak, C. E. Wright and G. R. Burket, Washington University, Seattle, *PB 147643*, Feb. 1960, 11 p. This program is a further modification of the non-symmetric correlation matrix programs reported previously. The essential new feature is the option of punching the sums, sums of squares and sums of cross products in a form which can later be added or subtracted, as well as reloaded, without additional IBM Type 533 panel wiring. By means of control cards, the following operations may be performed in any sequence: read case cards, punch summed quantities, add summed quantities, subtract summed quantities. 4 refs.

714 Multiple regression analyses program for the IBM Type 650. C. E. Wright, Washington University, Seattle, *PB 148732*, July 1959, 8 p. The program computes β matrices and multiple correlations according to the matrix equations $r_{nm}^{-1}T_{mn} = \beta_{mn}$ and $\beta_{nm}T_{mn} = R_{nn}$, where r_{nm} represents the intercorrelation matrix of predictor variables, T_{mn} a matrix of the correlations of the m predictor variables with the n criterion variables β_{mn} the m by n matrix of regression weights, and R_{nn} a matrix whose diagonal elements are the squares of the multiple correlations of the predictor variables with the criterion variables. 3 refs.

715 Wallops Island preliminary processing computer program. S. M. Ornstein, M.I.T., *PB 150795*, 25 July, 1960, 25 p.

See also:—

General, Ref. 626.

Mathematics, Ref. 692, 694, 700.

Analogue, Ref. 786.

ACCESSORIES

716 Analog-to-digital conversion with threshold detectors. P. W. Cheney, *IRE Trans. Electronic Computers*, **EC-10**, 100-101. In this letter, the relationship between logical complexity and conversion time is derived for a generalised, cascade, analogue-to-digital converter using threshold detectors for the digitising operation.

717 Analog to digital converter. J. Lettieri, *IBM Technical Disclosure Bull.*, **3**, Feb. 1961, 43-45. Description of a circuit, employing transistors and tunnel diodes, which operates on feedback and relative biasing principles to effect rapid conversion of analogue signals to digital form.

718 Computer generated displays. R. T. Loewe, R. L. Sisson and P. Horowitz, *Proc. IRE*, **49**, Jan. 1961, 185-195. This paper reviews techniques for performing two important functions in digital computer output display systems: digital-to-image conversion with symbol generation and generation of large, bright displays. The authors first review briefly various user requirements such as update response time, request response time, resolution, contrast, brightness, ambient illumination, fidelity, display and audience configuration, flicker rate, symbology, line drawings and formats. In a section on symbol generation, the topics discussed include dot pattern methods, scanning methods, waveform generators, beam shaping, line generation, and cathode ray tubes. The next section deals with projection displays and covers such subjects as silver halide photography, Kalfax photography, electrostatic techniques, Schlieren projection, light generation and colour, and electroluminescent panels. 52 refs.

719 Data communication. G. O. Vincent, *Data Processing* (Detroit), **3**, Feb. 1961, 7-12. An account of various Western Union communication systems for digital data.

720 The development of the flexible-disk magnetic recorder. R. T. Pearson, *Proc. IRE*, **49**, Jan. 1961, 164-174. This paper gives an account of the flexible disc magnetic recording system developed by Laboratory for Electronics, Inc. The flexible-disc recorder resulted from an approach to the problem of maintaining small, constant head-record separation by means of fixed heads which the recording medium dynamically approaches. Essentially, the recorder employs a flexible magnetic disc which rotates over a backplate in which heads are embedded flush with its surface. The effect of various constructional and operating features on the disc-backplate separation are discussed in detail. 8 refs.

721 Digital communications systems. H. Roth and R. J. Rosen, *Data Processing* (Detroit), **3**, Feb. 1961, 15-20. This article, in which the problems of digital data communications are discussed generally, consists of two parts. In **Part I—The parameters of the problem** by H. Roth (p. 15-18), the user's problem is examined to define those aspects of the operation and equipment which must be analysed to select the optimum system. **Part II—The equipment manufacturer attacks the communication problem** by R. J. Rosen (p. 18-20) considers the problems in developing input-output, transmission and switching equipment for digital data communications systems.

722 Digital data communication techniques. J. M. Wier, *Proc. IRE*, **49**, Jan. 1961, 196-209. In this paper, the major elements of digital data communication systems are identified and discussed and techniques currently employed or being developed for mechanising these elements are described and compared. A general account of the basic problem of digital data communication is followed by a section dealing with modulation and demodulation in which the following types of modulation are considered: voltage level, double-sideband amplitude, vestigial sideband, frequency, phase, and quadrature phase. The next section is concerned with noise, filtering, error control and coding. Other sections deal with synchronisation, switching and channels. Finally, information sources and sinks and overall systems are briefly discussed. 50 refs.

723 Message check character for serial transmission system. D. H. Rumble, *IBM Technical Disclosure Bull.*, **3**, Feb. 1961, 14-16. Description of a system in which a check character developed from the data characters of a message, depends upon the relationship between each character and its predecessor. It also cumulatively represents the number of times that bit positions remain one and the number of times that bit positions remain zero in successive message characters.

724 Permanent storage media. P. C. Constant, *Instr. & Control Systems*, **34**, Feb. 1961, 262-264. Brief review of media for the permanent storage of digital data. After brief mention of punched cards and paper tape, a general account is given of the factors affecting long term storage of magnetic tape. Finally, photographic systems under development are surveyed. 30 refs.

725 A squaring analog-digital converter. J. R. Cox, *IRE Trans. Electronic Computers*, **EC-10**, March 1961, 98-100. Letter describing, with logical diagram, how the square of a digital word can be obtained simultaneously with analogue-to-digital conversion by a modification of the trial encoder method of conversion.

726 Data handling for a research and developmental static test stand. T. Wong, Naval Ordnance Test Station, China Lake, California, *PB 152345*, 15 August 1960, 8 p. This report describes a data acquisition system for a static test complex. The system can measure phenomena from rocket motors having an average thrust of 1,000,000 pounds and a peak thrust of 10,000,000 pounds. The data measurement capacity is 200 channels. Discussion is concentrated on the technique of data handling and measurements, real time digitisation, automatic calibration and stored program data control. Included is a description of a new sampling technique for commutating multiple data channels. The sampling format is programmable and can be altered during a test according to existing conditions.

727 Errors in data transmission systems. R. G. Enticknap, M.I.T., *PB 152465*, 29 Sept. 1960, 17 p. This report is concerned with measurements in two main areas: the recording and analysis of errors in channels used for digital data transmission; and the recording and analysis of disturbances in circuits of the type used for data transmission. 4 refs.

728 The TX-2 electrostatic display system. R. E. Savell, M.I.T., *PB 152468*, 22 August 1960, 23 p. The display is produced in a 7-inch square on the face of an electrostatically deflected cathode ray tube. Ten bits are used in each axis to address the location of the spot to be displayed. The bits are decoded to produce the deflection voltages, and after a 7 microsecond set-up time, the spot is intensified for 10, 20, 40 or 80 microseconds according to instructions received from the computer. Work is in progress on a focus-correction circuit and on modifications to improve decoder stability. The display is used for visual observation, photographic observation with Polaroid 16mm or 35mm cameras, or photoelectric observation. For the latter, a photodiode mounted in a "light pen" is used to sense the display output. The light pen output can then be used to modify the computer program. The system can also be used as a flying spot scanner, with a photomultiplier replacing the light pen, to provide photographic and character recognition inputs to the TX-2. 1 ref.

729 Data transmission system. Decca Record Co., Ltd., *B.P. 860830*, 8 Feb. 1961. A system for the transmission of serial binary data has four channels. One channel is used for the transmission of the 1's and another for the 0's of odd digits (i.e. the first, third, fifth, etc., digits) and the remaining two channels are used for the 1's and 0's of the even digits.

730 Magnetic tape spool. Decca Record Co., Ltd., *B.P. 861053*, 15 Feb. 1961. A spool specially designed for magnetic data-recording tape, has a pin which resiliently engages in a radial slot in a spool flange to hold down the outer end of the wound tape.

731 Analogue-to-digital converter employing superconductors. Int. Business Machines Corp., *B.P. 861282*, 15 Feb. 1961. An analogue-to-digital converter employs a closed superconductive loop which includes hard and soft superconductors. Magnetic field producing input means is inductively coupled to the hard superconductor and output means responds to each change of state of the soft superconductor.

732 Magnetic head. Standard Telephones & Cables Ltd., *B.P. 861551*, 22 Feb. 1961. A magnetic head suitable for mass production and intended for use with magnetic drums, has a two-part core which is held in the head without screw connections.

733 Printer. Int. Business Machines Corp., *B.P. 861776*, 22 Feb. 1961. A printer designed for use with a data processor, employs hammers which are coupled to members selectively movable into engagement with a rotatable drum to effect printing by type faces on a driven endless band.

734 Magnetic tape transport system. Int. Business Machines Corp., *U.S.P. 2952010*, 6 Sept. 1960. A tape transport employing vacuum columns to produce tape motion and tape tension, is used to position successively sections of tape at rest around a rotating drum which carries magnetic heads.

735 Magnetic tape data recording system. National Cash Register Co., *U.S.P. 2954546*, 27 Sept. 1960. A particular data block is located on a tape by employing for control of the tape transport, the results of a comparison of addresses recorded on the tape with an address stored in a relay register.

736 Track selector for a magnetic record. Int. Business Machines Corp., *U.S.P. 2954547*, 27 Sept. 1960. Magnetic heads for different tracks of a disc or other record member are mounted for rotation together about a common axis and are orientated at different angles, so that any required head can be brought to operative position by such rotation.

737 Magnetic recording system. Int. Telephone & Telegraph Corp., *U.S.P. 2955280*, 4 Oct. 1960. This patent relates to a data recording system in which data recorded, on tape for example, with blank spaces between words is re-recorded without such spaces. This is achieved by means of delay lines and a recording arrangement which is driven at a fraction of the speed of the reading arrangement.

738 Error burst correction in digital transmission system. Bell Telephone Labs., Inc., *U.S.P. 2956124*, 11 Oct. 1960. Correction of error bursts in a digital data transmission system is effected with simplified circuitry in which encoding and decoding circuits, employing shift registers process data on a continuous basis

739 Digital-to-analogue converter. Sylvania Electric Products Inc., *U.S.P. 2956272*, 11 Oct. 1960. A digital-to-analogue converter using a saturated transistor as a no-gain switch to control an input reference voltage to an impedance network according to binary data of a flip-flop.

See also:—

General, Ref. 626.

ELEMENTS

740 Carry look-ahead adder. J. Earle and G. A. Maley, *IBM Technical Disclosure Bull.*, 3, Feb. 1961, 17-18. Description of an arrangement in which NOR blocks generate a carry look-ahead signal over two full adder circuits.

741 Computer memories: a survey of the state-of-the-art. J. A. Rajchman, *Proc. IRE*, 49, Jan. 1961, 104-127. This paper is concerned with high speed, random access memories or stores, normally in the form of arrays or matrices of storage cells, with a capacity in the range of one hundred to millions of words and an access time ranging from a fraction of a microsecond to tens of microseconds. Small capacity memories such as registers and memories such as discs, drums and tapes with relatively long access times are not covered. The purpose of the paper is to survey developments of the last decade, the present state and efforts for improvement. After a general consideration of storage and selection principles of random access memories, the major portion of the paper is devoted to magnetic memories and deals with such topics as principles and engineering considerations of current-coincident-driven core memories; magnetic decoding and load-sharing switches; word-organised one-core and two-core per bit memories; fast and impulse switching; transfluxor memories; nondestructive readout memories; ferrite apertured plates; twistors; fixed read-only memories; thin magnetic film memories—dots, sheets, coated wires and rods; present operational memories typically with capacities of 10^5 to 10^6 bits and read-write cycles of 2 to 15 μ sec; likelihood of the order of 100 nsec read-write cycle times attainable with ferrite and thin film memories; and considerations relating to large capacities. Short sections of the paper deal with ferroelectric, cryoelectric and tunnel diode memories. 96 refs.

742 The cryosistor—a new low-temperature three-terminal switch. I. Melngailis, *Proc. IRE*, 49, Jan. 1961, 352-354. Letter describing a low temperature device in which a reverse biased PN junction is used to control the ionisation between two ohmic contacts and which has promise as a fast monostable or bistable switch. 5 refs.

743 A digital static magnetic wire storage with nondestructive read-out. C. G. Shook, *IRE Trans. Electronic Computers*, EC-10, March 1961, 56-62. After a brief review of pertinent magnetic effects and sonic wave propagation in elastic media, a non-volatile, digital, magnetic storage scheme is described, wherein binary words may be stored by magnetising segments of a wire, and the information may be read out an unlimited number of times with no deterioration of the stored information by means of a stress wave created by magnetostriction. 18 refs.

744 Electrodeposited thin metallic film elements. J. C. Lloyd, R. S. Smith and R. G. Stevens, *IBM Technical Disclosure Bull.*, 3, Feb. 1961, 36. Brief description of a method of electroplating a thin magnetic film on a metal base which is removed after the film has been glued to a non-conducting substrate.

745 Electrodeposition of superconductive tin. I. Tsu, *IBM Technical Disclosure Bull.*, 3, Feb. 1961, 39-40. Description of a process employing an acid plating bath to prepare superconductive films of tin which adhere firmly to the substrate.

746 Esaki diode binary counter. A. J. Gruodis, *IBM Technical Disclosure Bull.*, **3**, Feb. 1961, 34-35. Description of a binary counter circuit having a switching section and a counting section, each of which employs an Esaki diode.

747 Esaki diode binary trigger. A. S. Myers, *IBM Technical Disclosure Bull.*, **3**, Feb. 1961, 32-33. Description of a binary trigger which is essentially a d.c. bridge employing Esaki diodes, resistors and inductors.

748 Etching Esaki diodes. E. M. Davis, *IBM Technical Disclosure Bull.*, **3**, Feb. 1961, 26-27. Brief description of apparatus for electrolytically etching an Esaki diode to obtain a specified current-voltage characteristic.

749 A function generator using cold-cathode selector tubes. R. M. Duffy and C. P. Gilbert, *IRE Trans. Electronic Computers*, **EC-10**, March 1961, 71-77. A method of generating voltages which are arbitrary functions of time is suggested in which a chain of cold-cathode selector tubes is used as a single pole, multi-position switch. A generator using this method is described in detail and typical output curves are given. The generator is extremely versatile, not only in a wide range of functions but also in the ability to operate over a wide range of speeds, change instantaneously from one speed to another, and generate two functions, one displaced with respect to the other by a variable, preset delay. 3 refs.

750 High-order probability generators. R. B. Stone and G. M. White, *IRE Trans. Electronic Computers*, **EC-10**, March 1961, 92-93. This letter refers to various methods of generating random numbers and describes a method of generating first and higher order sequences of binary digits at an 8 kc/s rate making use of Japanese magnetic-type parametrons. 6 refs.

751 Magnetic film memory design. J. I. Raffel, T. S. Crowther, A. H. Anderson and T. O. Herndon, *Proc. IRE*, **49**, Jan. 1961, 155-64. This paper is concerned with the design and manufacture of high speed, random access memories or stores employing thin magnetic films of permalloy. The properties of permalloy films and factors involved in their preparation by evaporation and electroplating are discussed. Engineering design is then considered with particular reference to the thin film memory which has been in operation in the control unit of the TX-2 computer at M.I.T. since the summer of 1959. This memory with destructive readout has a capacity of 32 ten-bit words and uses two 16×16 arrays of circular spots 1/16 inch diameter and about 700 Å thick. Emphasis is given to the selection system and the constraints which it imposes on film uniformity. Developments necessary to obtain higher speed and larger capacities are discussed; the main requirements are higher bit densities and improved techniques to minimise undesirable coupling between drive and sense lines. It is suggested that the use of 10×60 mil rectangles, balanced sense windings and longer words should permit memories of about 200,000 bits with cycle time under 0.2 µsec. 22 refs.

752 A 6-megacycle cryotron ring oscillator. M. L. Cohen, *Proc. IRE*, **49**, Jan. 1961, 371-372. Letter describing a 6 Mc/s cryotron ring oscillator made possible by better film cryotrons resulting from improved evaporation techniques. (See the paper abstracted in *C.A.*, **5**, March 1961, Ref. 532).

753 Multipath logic circuits. H. Mathers, *IBM Technical Disclosure Bull.*, **3**, Feb. 1961, 38. Brief description of the application to OR or NOR logic functions of a magnetic core provided with two additional holes for that purpose.

754 Switching circuit with local bias. C. E. Dorrell and G. A. Newman, *IBM Technical Disclosure Bull.*, **3**, Feb. 1961, 31. Brief description of a circuit in which one of the bias sources of an inverter is augmented by a rectified a.c. signal fed through a saturable core transformer. This produces a bias voltage "outside" of the voltages available. Thus, voltage saturation occurs at one voltage extreme while current saturation exists at the opposing voltage extreme.

755 Investigations in digital technology research. G. Estrin, C. Leonides et al., California University, *PB 152213*, May 1959, 186 p. This report is concerned with the measurement of properties of magnetic materials as a function of temperature, the measurement of magnetic properties of thin films, and the system evaluation and experimental investigation of a modified form of the twistor. 13 refs.

756 Research on magnetic rod storage and switching device. A. J. Kolk, Nat. Cash Register Co., *PB 152520*, 31 July 1960, 105 p. This report presents the results of a study concerned with the magnetic properties of thin film, iron-nickel alloys electrodeposited in a rod configuration. These properties were found to be critically influenced by the physical condition of the conducting substrate surface. Silvered-glass and beryllium-copper substrates were subjected to intensive investigation. The effects of varying other plating parameters such as current density, pH, bath composition, temperature, organic additives, plating time, and the presence of an axial magnetic field were also studied. Electron micrographs were made of the substrate surface and the plate at different plate thicknesses. An attempt was made to correlate residual stress measurements with the properties of the plate. Preferred orientation in the plate was investigated by means of X-ray diffraction techniques. A series of experimental switching curves were determined and a mechanism for the switching phenomena proposed. 18 refs.

757 Register. Int. Business Machines Corp., *B.P. 860007*, 1 Feb. 1961. This patent concerns a register composed of storage elements, such as piezoelectric or ferroelectric elements, arranged in a matrix with equal numbers of columns and rows. Input means for each column and output means for each row are energised by drive means for groups of elements, each group comprising an element in each row but no two elements in the same column.

758 Capacitor data storage. Int. Business Machines Corp., *B.P. 860483*, 8 Feb. 1961. A data storing capacitor is provided with circuit arrangements for maintaining the charge on the capacitor during a readout interval.

759 Switching circuits. Standard Telephones & Cables Ltd., *B.P. 861124 & 861125*, 15 Feb. 1961. *B.P. 861124* describes an AND or OR circuit comprising a magnetic core having input windings and a bias winding and arranged so that only in the absence of all input pulses is a pulse produced in an output winding. *B.P. 861125* concerns an AND circuit comprising a (non-exclusive) OR circuit with inputs and output connected to inverter circuits.

760 Superconductive element. Int. Business Machines Corp., *B.P. 861280*, 15 Feb. 1961. A thin superconductive film is provided on one side with a drive winding and on the other side with a sense winding.

761 Superconductive element. Int. Business Machines Corp., *B.P. 861281*, 15 Feb. 1961. A superconductive film has an aperture bounded in part by an integral bridge portion adjacent which are drive and sense conductors; insulating means are arranged so that there is better thermal conductance between the sense conductor and the film than there is between the drive conductor and the film.

762 Magnetic core matrix. Int. Business Machines Corp., *B.P. 861328*, 15 Feb. 1961. This patent is concerned with a modification of the magnetic core matrix described in *B.P. 854380 (C.A.)*, **5**, Jan. 1961, Ref. 123) for use where storage and readout is always in words of a given size; groups of column conductors are connected to associated switches arranged in a matrix.

763 Transistor counter. Gen. Electric Co., Ltd., *B.P. 861509*, 22 Feb. 1961. In a binary counter comprising bistable stages each of two cross-connected transistors, the input is connected to each transistor of each stage by way of an associated gate controlled according to the condition of that stage and lower stages.

764 Shift register. Siemens & Halske A.-G., *G.P. 1097725*, 19 Jan. 1961. This patent is concerned with a shift register employing magnetic cores, which is designed so that only two windings are required per core.

765 EXCLUSIVE-OR gate. Siemens & Halske A.-G., *G.P. 1098033*, 26 Jan. 1961. A circuit for an EXCLUSIVE-OR gate employs two transfluxors.

766 Inverter. Int. Business Machines Corp., *U.S.P. 2951953*, 6 Sept. 1960. This patent describes an inverter circuit which makes use of a transistor and a Zener diode.

767 Shift register. North American Philips Co., Inc., *U.S.P. 2952009*, 6 Sept. 1960. A shift register employing magnetic cores is designed so as to require fewer windings on the cores.

768 Parallel binary accumulator. Nat. Cash Register Co., *U.S.P.* 2952407, 13 Sept. 1960. An accumulator which adds a binary number to its contents in response to a single actuating pulse, is provided with a logical network which determines all the inter-stage carry information prior to the setting up of the new sum.

769 Analogue multiplier. H. B. O. Davis and R. A. Meyers, *U.S.P.* 2952408, 13 Sept. 1960. This patent is concerned with the circuit design of a four-quadrant electronic multiplier having good stability coupled with high accuracy.

770 Universal logic block. Int. Business Machines Corp., *U.S.P.* 2952792, 13 Sept. 1960. A universal logic block for signalling the occurrence of a selected one of 2^n possible functions of n variables, comprises a specified arrangement of n groups of paired complementary variable switching elements, the 2^n switching elements in group n being each shunted by one of 2^n function switching elements. The particular block described in this patent employs photoconductive and electroluminescent elements.

771 Shift register. Radio Corp. of America, *U.S.P.* 2953755, 20 Sept. 1960. A shift register employing magnetic cores, is provided with transfer circuitry designed so that each core requires only two windings.

772 Binary counter. Burroughs Corp., *U.S.P.* 2954163, 27 Sept. 1960. A binary counter employs transistors coupled by circuits each including a transformer and a capacitive-resistive differentiating network.

773 Adder-subtractor. Philco Corp., *U.S.P.* 2954168, 27 Sept. 1960. The circuit of a parallel binary adder-subtractor is designed for reduced carry propagation time, stages being arranged in groups in which the carry is simultaneously indicated.

774 Flip-flop. Gen. Precision Inc., *U.S.P.* 2954484, 27 Sept. 1960. A flip-flop circuit employs two, directly-coupled transistors.

775 Bistable circuit. Laboratory for Electronics Inc., *U.S.P.* 2955211, 4 Oct. 1960. A bistable circuit, employing a magnetic core and a single resistively-gated transistor, is designed for low power requirements and relatively high speed.

776 Accumulator. Kienzle Apparate G.m.b.H., *U.S.P.* 2955759, 11 Oct. 1960. An accumulator employing magnetic core registers, is designed to facilitate shifting.

777 Counter. Int. Business Machines Corp., *U.S.P.* 2956155, 11 Oct. 1960. A circuit for a counter employs only one triode or other electron discharge device and one gas discharge diode per stage.

778 Transistor gate. Radio Corp. of America, *U.S.P.* 2956175, 11 Oct. 1960. A circuit for a gate, operating at high speed with relatively low input signal levels, employs a transistor, coupled as a common base amplifier, which is gated by an auxiliary transistor directly coupled in series with the base lead of the common base amplifier.

779 Fast carry counter. Sperry Rand Corp., *U.S.P.* 2956181, 11 Oct. 1960. This patent describes a circuit for a parallel, fast carry, binary counter with serial carry gate propagation.

780 Half adder. Sperry Rand Corp., *U.S.P.* 2956182, 11 Oct. 1960. This patent presents a simple design for a half adder, which may be implemented with direct coupled transistor logic or resistor coupled transistor logic.

781 Counter. Burroughs Corp., *U.S.P.* 2956745, 18 Oct. 1960. A counter is described which employs magnetic cores in a shift register and a logic network connected to form a closed loop.

782 Subtractor. Bell & Howell Co., *U.S.P.* 2956748, 18 Oct. 1960. A pulse generator supplies pulses to two counters and is controlled by a binary switch to which is coupled the recycling pulse output of one counter so that the number stored in that counter is subtracted from the number stored in the other counter.

783 Ferroelectric data storage circuit. Bell Telephone Labs. Inc., *U.S.P.* 2957164, 18 Oct. 1960. A circuit employing a ferroelectric capacitor for data storage, is designed for high speed and non-destructive readout.

784 Shift register. Sperry Rand Corp., *U.S.P.* 2958075, 25 Oct. 1960. An inexpensive, rugged shift register employs magnetic amplifiers as basic components and is designed for shifting to right or left and for serial or parallel readin and readout.

See also :—

General, Ref. 626.

ANALOGUE

785 The development of the modern digital differential analyser. G. C. Rowley, *Automn. Progress*, 6, March 1961, 82-88. Accounts are given of the historical development and operation of analogue and digital computers, followed by an account of the development of the digital differential analyser and its applications. 1 ref.

786 A new active-passive network simulator for transient field problems. W. J. Karplus, *Proc. IRE*, 49, Jan. 1961, 268-275. This paper describes the design, operation and application of a computer, called the discrete-space-discrete-time (DSDT) computer, which is the result of a hybridisation of analogue and digital techniques. A wide variety of problems characterised by partial differential equations can be simulated by means of a network consisting only of positive and negative resistors. No reactors are used, the negative resistors being realised with the aid of d.c. amplifiers. Unlike conventional analogue methods, the time as well as the space variables are approximated by finite difference expressions; thus the solution proceeds stepwise in time as on a digital computer. Only implicit difference equations are instrumented, so that there is no danger of computational instability no matter how large the time increment. Among the field problems which can be treated by this computer are problems characterised by the diffusion equation, the wave equation, the biharmonic (beam) equation, and various modified forms of these equations. 3 refs.

787 Special purpose analogue computer. Garrett Corp., *U.S.P.* 2955761, 11 Oct. 1960. This patent describes an electronic analogue computer designed to solve an equation in which an unknown variable occurs in the second power; it is particularly intended for computing certain aeronautical data such as the angle of attack, angle of yaw, the true air speed of an aircraft and the relative density of the ambient air.

DIGITAL

788 From the Philco 2000 Series—the 212. R. E. Steele and R. A. Groton, *Datamation*, 7, Feb. 1961, 24-27. General description of the Philco 212.

789 Logical design of CG24 (a general-purpose computer). G. P. Dinneen, J. A. Dumanian et al., *M.I.T.*, *PB 148281*, 15 April 1957, 47 p. A detailed design is presented for a high speed, general purpose digital computer. The design considerations are governed by the assumption that implementation of the machine is to be accomplished using only solid state devices. This report describes the essential characteristics, structure and method of design of the computer and discusses its detailed logical structure.

790 Digital computer with program interruption arrangements. Nat. Research Development Corp., *B.P.* 861190, 15 Feb. 1961. This patent is concerned with a digital computer which has arrangements for interrupting a program when an instruction word is reached that contains a group of digits previously set up by switches.

791 General purpose computer. Nat. Cash Register Co., *U.S.P.* 2954166, 27 Sept. 1960. This patent provides a comprehensive description of a large scale, magnetic drum computer.

See also :—

General, Ref. 623.

Analogue, Ref. 786.

PROGRAMMING

792 COBOL and compatability. H. Bromberg, *Datamation*, 7, Feb. 1961, 30-34. After brief outlines of the development and structure of COBOL, an account is given of a demonstration of compatability at which two COBOL programs were compiled and run using both the UNIVAC COBOL Compiler and the RCA 501 COBOL Narrator.

793 The evolution of programming systems. W. Orchard-Hays, *Proc. IRE*, **49**, Jan. 1961, 283-295. This paper surveys and summarises programming developments in recent years and draws some general conclusions as to trends in techniques and principles. Topics which are discussed include: preparation and use of computer routines; assemblers; organisational compilers; mathematical formula compilers; programming systems for data processing applications; information storage and retrieval programming systems; simulation programs; specialised programming systems for specific problems such as linear programming computations; list processors; general systems for operating computers; dual master-operating systems (self-updating master system and an operating system which is a by-product of a compile run); and processor compilers (compiler for writing compilers). 16 refs.

794 Program Supervisor. K. Maling, *IBM Technical Disclosure Bull.*, **3**, Feb. 1961, 12-13. Brief description of how program debugging is expedited by maintaining a count of instructions and employing a supervisory program to interpret program errors in the light of the instruction count.

795 The programmer's task. J. F. Davison, *Auto. Data Processing*, **3**, Feb. 1961, 35-38, 46. Condensed from a chapter of the author's book *Programming for digital computers* (See C.A., **5**, March 1961, Ref. 620).

See also:—

General, Ref. 627.

Techniques, Ref. 704, 708.

APPLICATIONS

AERONAUTICAL

796 Data collecting and processing at the Pacific Missile Range. R. E. Stockwell, *Automn. & Auto. Equipment News*, **6**, Feb. 1961, 306-310. General account of the new Pacific Missile Range in California operated by the U.S. Navy and its data collecting and reducing equipment which includes an IBM 709.

797 Digital computer equipment for an advanced bombing, navigation and missile guidance subsystem for the B-70 air vehicle. T. B. Lewis, *Proc. IRE*, **49**, Jan. 1961, 313-318. General account of the transistorised, high speed, general purpose digital computing equipment designed as the primary airborne real time calculating element for the advanced bombing, navigation and missile guidance subsystem intended for use in the B-70 air vehicle. Reliability, maintainability and flexibility received the utmost consideration in every design phase. Maximum reliability was achieved primarily through the use of a powerful, versatile, parallel main computer section supported by a minimal serial, emergency computer. A new approach to fault location enhances computer maintainability and permits in-flight repair, while flexibility is achieved by means of unique, high speed input-output processing equipment.

798 Flow properties of an unyawed 10-deg cone for $\gamma = 1.28$ to 1.40 at Mach numbers of 1.5 to 8. W. T. Strike and B. B. Norton, Arnold Engineering Development Center, *PB 152260*, Oct. 1960, 81 p. Numerical solutions for a nonlinear differential equation proposed by G. I. Taylor and J. W. Maccoll to describe the flow about a cone were carried out on an IBM 704 for variable ratios of specific heats. The solutions were obtained for an unyawed 10-deg semi-angle cone at $\gamma = 1.40, 1.36, 1.32$ and 1.28 at Mach numbers within the range of 1.5 to 8.24. 2 refs.

799 Membrane theory of large spherical radomes. A. L. M. Grzedziński, National Research Laboratories, Canada, *PB 152832*, May 1960, 83 p. Two methods of stress analysis of large spherical radomes are developed: an elementary desk calculator analysis, based on the restrictive assumption of air-load being axially symmetric with respect to the wind direction, and a general unit load method, making use of a medium size digital computer. Both methods account for an elastic support at the foundation. 14 refs.

800 Numerical investigations on the solution of the non-linear equation of supersonic flow by finite difference methods (Part II). G. Seegmüller, Technische Hochschule, Munich, *PB 152492*, 25 July 1960, 29 p. This report contains a proof of a theorem which establishes the local existence and uniqueness of the solution of the difference equations resulting from a mean-value approximation and secures the convergence of a certain Newton sequence. Information is given on finding the true solution by extrapolation on a sounder basis. There is a discussion on streamline-integration. 2 refs.

801 A prototype high speed digital system for hotshot tunnels. G. E. Gilley and M. L. Bunn, Arnold Engineering Development Center, *PB 152555*, Oct. 1960, 45 p. A prototype high speed digital system for obtaining a large amount of raw data in a form for reduction by digital computers, has been built and tested in two arc-discharge wind tunnels. The system is used in conjunction with a carrier-amplifier and recording oscillograph system to obtain digital data in parallel with the analogue data. A high speed electronic commutator switches the analogue signals into an analogue-to-digital converter. The digital data is stored in a magnetic core store and later transferred to paper tape. 2 refs.

See also:—

Analogue, Ref. 787.

Miscellaneous, Ref. 833.

BUSINESS

802 ADP is on the agenda in the insurance industry. K. Bean, *Auto. Data Processing*, **3**, Feb. 1961, 16-18. Brief historical account of the use of punched card and other business machines by British insurance companies and discussion of the problems involved in conversion to computers.

803 The Cooperative that coordinated. G. Thorne, *Auto. Data Processing*, **3**, March 1961, 12-15. General account of a punched card system, in which use is made of a tabulator linked to a GAMMA 3 magnetic drum computer, employed for branch invoicing and stock control by a large French chain store group, the Coopérative Régionale des Charentes et du Poitou.

804 Fourteen-computer net to speed data flow. M. Murphy, *Control Engng.*, **8**, March 1961, 40, 42. Brief account of how Hughes Aircraft Company are to use fourteen IBM 1401 computers, each in a separate division of the company, as satellites of a central IBM 7090 for product definition, material control, fabrication and assembly scheduling control, finished inventory and shipping, and manufacturing cost accumulation.

805 Lifemanagementship. K. Bean, *Auto. Data Processing*, **3**, March 1961, 29-32. Brief accounts of computer systems to be used by three insurance companies for processing ordinary life policy transactions: London and Manchester Assurance Co.—PEGASUS; Prudential Assurance Co.—ORION; and Royal London Mutual Insurance Society—IBM 1401.

806 Pioneering experience. K. Bean, *Auto. Data Processing*, **3**, Feb. 1961, 19-21. Account of the experience of the Legal and General Insurance Company in applying a National-Elliott 405 to group life and pension schemes.

807 Q: When is an order clerk redundant? A: When you have a computer. H. G. Johnston and C. A. Pursley, *Auto. Data Processing*, **3**, March 1961, 16-17. Brief description of how the inventory control system employing an IBM 705, at the Transformer Division of Westinghouse Electric Corporation, has been modified so that purchase orders are automatically typed when required.

808 Trading stamps bow to automatic data processing system. M. Reid, *Control Engng.*, **8**, March 1961, 32, 35. Brief account of an automatic data processing system to be used by American Premium Systems Inc., which will enable customers to be awarded premiums without collecting trading stamps and pasting them in books. In this system, a retailer sends details of points earned by a customer to a centralised data processing centre where they are stored on magnetic tape. The tapes are updated weekly with an IBM 7074 (faster version of the IBM 7070) which produces a tape containing details of customers with a total of 1,500 points. This tape is run monthly through an IBM 1401 which prepares vouchers which can be redeemed for goods.

See also:—

Miscellaneous, Ref. 833.

CONTROL—GENERAL SYSTEMS

809 Computers in automatic control systems. J. G. Truxal, *Proc. IRE*, **49**, Jan. 1961, 305-312. This paper discusses the developments in automatic feedback control systems made possible by the integration of a computer into a system. The paper has three main sections dealing with the control of complex systems, adaptive control and optimising control. In each section an attempt is made to delineate the class of control problems which become amenable to solution when computers are admitted as control elements and the requirements placed on the computer and probable future directions of development are discussed. Examples are given of current applications of computer-control concepts. 11 refs.

CONTROL—PRODUCTION AND PROCESS

810 **Computer scorecard.** *Control Engng.*, 8, March 1961, 97, 99. A list of 31 closed-loop control installations employing digital computers in the steel industry, chemical and petroleum processing plants and electric power stations.

811 **An adaptive system using periodic estimation of the pulse transfer function.** S. Bigelow and H. Ruge, Columbia University, *PB 162253*, 30 June 1960, 34 p. The purpose of the investigation described was to gain insight into the behaviour of adaptive control schemes by studying in detail a particular plant-adaptive control system. In connection with this work a general purpose digital computer was used for experimental simulation. The system considered may be described in terms of two basic blocks, the plant and the control computer. The control computer is a digital device, and as such its inputs and outputs are inherently sampled signals. It is convenient, therefore, to treat the entire system as a sampled data system. The plant or process to be controlled is assumed to be a continuous, low-pass linear but time-varying dynamic system, and to include a zero-order hold which converts the sampled input to a piecewise-constant signal. The control computer serves two basic purposes. First from samples of the plant input and output it computes periodically a statistical estimate of the plant pulse transfer function. Second using the current estimate of the dynamic behaviour of the plant and measurements of system input (set-point) and output, the plant input is computed in accordance with a suitable overall performance criterion. This general scheme of plant-adaptive control obtains information about the current dynamics of the plant from measurements of normal plant input and output alone. 7 refs.

See also :—

Techniques, Ref. 702, 704.

Business, Ref. 804.

Miscellaneous, Ref. 833, 835.

ELECTRONICS

812 **Computer design of multiple-output logical networks.** T. C. Bartee, *IRE Trans. Electronic Computers*, EC-10, March 1961, 21-30. This paper presents a procedure for the design of multiple-output logical networks which are minimal according to certain criteria. The technique has been programmed for the IBM 709 and some of the details of the program are presented. The program accepts punched cards listing the in-out relations for the network, and then prints a list of Boolean expressions which are minimal according to a selected one of three criteria. 11 refs.

813 **Digital simulation in research on human communication.** E. E. David, *Proc. IRE*, 49, Jan. 1961, 319-329. This paper is concerned with investigations of communication systems using digital simulation and involving pictorial matter and speech which have been carried out at Bell Telephone Laboratories. Principally, the investigations concerned codings aimed at conserving transmission channel capacity. Closely related are investigations aimed both toward automatic recognition of perceptual attributes of signals, and psychological investigation of perceptual mechanisms. The paper briefly describes some of the studies and the techniques developed for attaining realistic, workable simulations. 23 refs.

814 **Research services on moving-target indication.** A. Nirenberg, E. Letscher and P. Seckendorf, Airborne Instruments Laboratory, *PB 148711*, March 1960, 177 p. An accurate, high rate, digital radar data recording and handling system is described. The system was designed to gather data on the physical and statistical characteristics of radar ground clutter; this information will be used to provide a basis for developing new and improved techniques and circuitry for MTI radar systems. Each of eight discrete parameters describing a single radar target can be quantised into an 11-bit binary number (each radar repetition period) and recorded on magnetic tape. This data is transferred to punched paper tape and made available in a form suitable for the Eckhart Mauchly digital computer, which calculates such clutter characteristics as signal time functions, correlation functions, and probability distributions. 10 refs.

See also :—

Techniques, Ref. 705.

Miscellaneous, Ref. 833.

ENGINEERING, CIVIL

See :—

Miscellaneous, Ref. 833.

ENGINEERING, ELECTRICAL

815 **Generating-station computer economics.** R. A. Baker, *Instr. & Control Systems*, 34, Feb. 1961, 250. Financial savings which might be obtained with a specified type of computer control of power stations are summarised.

Computer Abstracts, April, 1961

INFORMATION RETRIEVAL

816 **A classification system for any data banking (information storage and retrieval) process.** P. Garrett, Benson-Lehner Corp., *PB 148977*, 15 June 1959, 11 p. A study was started to discover and state explicitly the fundamentals of data banking (more commonly called information storage and retrieval). A logical framework of hierarchical tree, based on the organisation of the store and the method of search, is displayed that includes all possible data banking processes and shows their similarities and differences.

MECHANICAL TRANSLATION

See :—

General, Ref. 626.

Miscellaneous, Ref. 833.

NUCLEAR

817 **Digital computers monitor nuclear steam generator.** J. Auricoste, R. Chambolle, Y. Panis and J. Prades, *Control Engng.*, 8, March 1961, 127-131. The Chinon nuclear power plant of Electricite de France uses a gas cooled reactor with heat transfer from the carbon dioxide coolant to raise steam that drives turbine generators. Each of the reactor's 1,148 fuel cartridges has a magnesium alloy cladding. Because these elements operate near their critical temperatures, there is a strong possibility that the cladding may crack and release radioactive fission gas into the cooling system with possible permanent contamination of the reactor. This article describes a digital computer system for detecting pinhole leaks as they occur. To improve reliability, two RW-300 computers are employed, one acting as a stand-by. Essentially, the monitoring system selects a sample of gas from one group of four adjacent coolant channels, directs the sample through a complex valve arrangement to a coarse scaler in which two radiation measurements are made, and calculates from these measurements the fission gas activity change rate. 4 refs.

818 **Cloud—An IBM 709 program for computing gamma-ray dose rate from a radioactive cloud.** D. S. Duncan, Atomics International Div., North American Aviation Inc., *NAA-SR-Memo-4822*, 1959, 93 p.

819 **CRUNCH—An IBM-704 code for calculating successive first-order reactions.** M. P. Lietzke and H. C. Claiborne, Oak Ridge National Laboratory, *ORNL-2958*, Nov. 1960, 46 p.

820 **EQUIPOISE—An IBM-704 code for the solution of two-group, two-dimensional, neutron diffusion equations in cylindrical geometry.** M. L. Tobias and T. B. Fowler, Oak Ridge National Laboratory, *ORNL-2967*, 87 p.

821 **A preliminary study of the dynamics of solvent extraction cascades. I. Program for digital and analog simulation.** O. L. Updike and M. E. Whatley, Oak Ridge National Laboratory, *CF-59-9-47*, Sept. 1959, 23 p.

822 **Program for computing minimum critical sphere radii for uranium salts.** T. B. Patterson, Goodyear Atomic Corp., *GAT-DM-792*, Nov. 1959, 5 p.

823 **Scintillation counter γ —spectra unfolding code for the IBM-650 computer.** H. I. West and B. Johnston, University of California, *UCRL-5808*, Feb. 1960, 26 p.

824 **The study of multi-region reactions with an analog computer.** J. C. Peden, Hanford Atomic Products Operation, *HW-65578*, July 1960, 50 p.

See also :—

General, Ref. 626.

PHYSICS

825 **The calculation of transient temperature distributions in a solid cylindrical pin, cooled on the surface. IBM-704 program 524/RE-147.** J. Heestand et al., Argonne National Laboratory, *ANL-6237*, Oct. 1960, 140 p.

826 **PUBCO-II an IBM 704 code for computing the ideal thermodynamic functions of a diatomic gas molecule.** L. R. Sitney, University of California, *LA-2304*, March 1959, 82 p.

827 **The spectra of nitrogen oxides. II. The Urey-Bradley force constants in N_2O , and the infrared spectrum of solid $N_2^{15}O$.** I. C. Hisatsune, Kansas State University, *PB 148716*, Feb. 1960, 51 p. An IBM 650 has been programmed for the calculation of the force constants of dinitrogen tetroxide. 29 refs.

828 **WAT: A numerical method for two-dimensional unsteady fluid flow.** W. B. Goad, University of California, *LAMS-2365*, Sept. 1960, 21 p.

See also :—

Mathematics, Ref. 695.

SIMULATION

829 **Initial conditions in computer simulation.** K. S. Miller and J. B. Walsh, *IRE Trans. Electronic Computers*, **EC-10**, March 1961, 78-80. In this paper a technique is presented for the straightforward analogue simulation of the transfer function of a certain class of linear systems, in which the effects of both forcing function and initial conditions are determined simultaneously. The method is particularly well adapted for the analysis of systems with fixed transfer function and variable initial conditions and forcing functions. 6 refs.

830 **Simulation Council Newsletter.** J. H. McLeod (ed.), *Instr. & Control Systems*, **34**, Feb. 1961, 267, 269-277. Consists mainly of accounts of two Simulation Council meetings. From the Eastern Simulation Council meeting of 15 August 1960, the whole of a paper "The GE-MSVD combined analog-digital computer system" by M. Paskman is given together with summaries of "DDA considerations in combined computation" by R. J. Leake and "Some insight into time scaling" by J. Port. From the Central Simulation Council meeting of 19 September 1960, summaries are given of "The effects of second-order kinetics on chemical reactor control" by L. H. Fricke, "Nonlinearities in the Mercury Capsule heat transfer problem" by M. S. Fineberg and a discussion on nonlinear simulation.

TRANSPORT

831 **Computer controls air traffic.** *International Electronics*, **1**, March 1961, 44-45, 51. General account of the Volscan system developed by Avco-Crosley for the automatic talk down of aircraft. In this system, a computer supplied with radar information assemblies, from pre-recorded landing orders, coherent instructions which are transmitted to the aircraft.

832 **'Just one moment, sir while I ask the computer.'** P. W. Black, *Auto. Data Processing*, **3**, Feb. 1961, 26-28. Brief, general account of the automatic seat reservation system incorporating a computer used by Scandinavian Airlines System and developed by Standard Elektrik Lorenz.

See also :—

Miscellaneous, Ref. 833.

MISCELLANEOUS

833 **Advanced computer applications.** W. F. Bauer, D. L. Gerlough and J. W. Granholm, *Proc. IRE*, **49**, Jan. 1961, 296-304. This paper reviews applications which promise to become important commercially, as well as many which are simply interesting and unusual; in general, the well-established scientific and business applications are omitted. The main sections of the paper are: Literature and the arts (teaching, school timetable preparation, training, preparation of concordances, music, design of weaving patterns); Applications in medicine (diagnosis, analysis of measurements); Business and government (simulation of emergency duties of U.S. President, election forecasting, PERT for evaluation of progress of Polaris project, highway construction, assignment of telephone facilities, road traffic analysis, legal applications, analyses of chemical and sociological structures, generation of combinations of keys, gambling applications, salary recommendations); On-line applications (SAGE and other military applications, airline reservation systems, air traffic control, checking complex electronic systems, train control, control of ships through the Panama canal, space technology); Computers in communications (speech compression, message switching); Automobile traffic control (control of traffic signals); Language translation; and Process control. 54 refs.

834 **Analysis of research data.** *Data Processing* (Detroit), **3**, Feb. 1961, 30-32, 34. Consists of brief descriptions of three applications of the UNIVAC 1105 at the University of North Carolina Computation center:

- Urban studies program.** (p. 30-31). Data processing and problem solving for a research study of the impact of urbanisation in a particular area.
- Metropolitan measure.** F. E. Ashby. (p. 31-32). Computations for the ranking of American cities by metropolitan function as determined by data collected for six characteristics: wholesale sales, number of branch offices, business service receipts, retail sales, value added by manufacture, and bank debts.
- Textile research.** P. Keeney. (p. 34). Analysis of data to determine the relation of selected fibre properties of raw cotton to product quality and end-product performance.

835 **The computer as a component.** M. Palevsky, *Instr. & Control Systems*, **34**, Feb. 1961, 248. Briefly captioned block schematic diagrams showing the use of a Packard Bell PB 250 in a plotting system, process control, data gathering systems, and automatic checkout system.

836 **Computer model of gambling and bluffing.** N. V. Findler, *IRE Trans. Electronic Computers*, **EC-10**, March 1961, 97-98. Letter presenting a flow chart for a poker-playing program, which is under construction. 8 refs.

837 **Current trends in automated tutoring and their implications for naval technical training.** G. L. Bryan and J. W. Rigney, University of Southern California, *PB 152164*, Dec. 1959, 52 p. Teaching machines, computer-controlled teaching machines and computer-facilitated systems training are discussed in terms of the research being done and the applications now in existence. Comments are presented regarding some futuristic conceptions of automated training. The implications of these technological advances for increasing the efficiency of technical training in electronics are explored for individual and systems training. It is concluded that the appropriate role of teaching machines would be as supplements to conventional methods. Completely automated systems training is clearly unrealistic for present-day tactical data processing systems, but the central control computers in these systems do offer possibilities for advance in the art of systems training that should be taken into consideration and planned for in the design of systems training facilities. 13 refs.

838 **An IBM Type 650 program to summarize multiple criteria data on academic achievements.** C. E. Wright, G. E. Roudabush and G. R. Burket, Washington University, Seattle, *PB 148723*, June 1959, 49 p. This report is concerned with an IBM 650 registration system, adopted by the University of Washington Registrar's office, which makes it possible to summarize credits and grade points for individual students in 50 or more course areas. 4 refs.

See also :—

General, Ref. 626.

BOOKS

839 **Digital computer and control engineering.** R. S. Ledley, McGraw-Hill, 1961, 835 p., £5. 12. 6. "This book provides a unified treatment of all phases of digital computer engineering, from the basic electronic design of digital circuits to advanced automatic programming techniques. A functional approach to systems design utilizing numerical analysis and data handling methods is offered as a basis for the systems design of general and special purpose computers. Foundations for the logical design of digital circuitry are based upon the principles of Boolean algebra and numerical treatment of logic. Techniques of electronic design using semiconductor devices and magnetic elements are presented, and, as a concrete illustration, the detailed design of an entire general purposes computer [the Pedagogac] is developed from start to finish." (From publisher's announcement). Contents: Part 1 Introduction to digital programmed systems—Applications of digital computers and control, Principles and block diagram of a digital computer, Coding and programming a digital computer, Programming fundamentals, Advanced programming; Part 2 Functional approach to systems design—Fundamentals of numerical analysis, Searching, sorting, ordering and codifying, Special-purpose, digital-computer systems design, Systems design of the Pedagogac; Part 3 Foundations for the logical design of digital circuitry—Introduction to Boolean algebra and digital-computer circuits, The designation numbers and the design of function circuits, Elementary computational methods in circuit design, Boolean matrix equations and the fundamental formulas, Applications of matrix equations in circuit design; Part 4 Logical design of digital-computer circuitry—Serial arithmetic operations, Parallel and rapid arithmetic operations, Control, Packaging and the logical design of the Pedagogac; Part 5 Electronic design of digital circuits—Problems and limitations in electronic realization, Semiconductor elements in digital-circuit design, Magnetic elements in digital-circuit design, Memory and input-output methods, The electronic design of the Pedagogac.

